7.5W High-Integration, High-Efficiency PMIC for Wireless Power Transmitter

FEATURES

- VIN Input Voltage Range: 4V-6V
- Up to 7.5W Power Transfer
- Integrated Full-Bridge Power Stage with 20mΩ Rdson of Power MOSFETs
- Integrated 4.85V-65mA LDO
- Optimized for EMI Reduction
- Integrated Lossless Input Current Sensor with ±2% accuracy for FOD and current Demodulation
- Integrated voltage and current demodulation
- 3.3V and 5V PWM Signal Logic Compatible
- Input Under-Voltage Lockout
- Over Current Protection
- Over Temperature Protection
- 2mm*2mm QFN-18L Package

APPLICATIONS

- WPC Compliant Wireless Chargers of 5W or 7.5W Systems for Watches, Mobiles or other Wearable Devices
- General Wireless Power Transmitters for Consumer, Industrial and Medical Equipment
- Proprietary Wireless Chargers and Transmitters

DESCRIPTION

The SCT63042 is a highly integrated power management IC allows achieving high performance, high efficiency and cost effectiveness of wireless power transmitter system compliant with WPC specification to support up to 7.5W power transfer, working with a wireless application specific controller or a general MCU based transmitter controller.

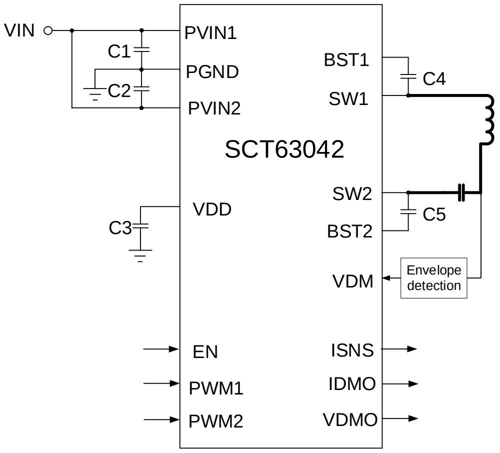
This device integrates a 4-MOSFETs full bridge power stage, gate drivers, a 4.85V LDO, communication demodulator and input current sensor for both system efficiency and easy-to-use.

The proprietary gate driving scheme optimizes the performance of EMI reduction to save the system cost and design. The proprietary lossless current sensing circuitry with ±2% accuracy monitors input current of full bridge to support Foreign Object Detection FOD and current demodulation. The build-in 4.85V low dropout regulator LDO can provide power supplies to transmitter controller and external circuitries.

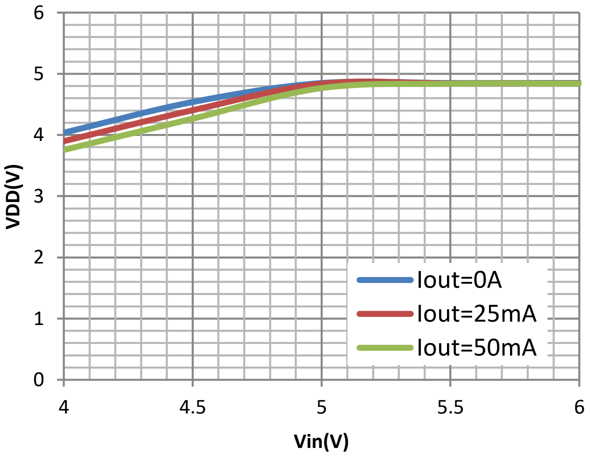
The SCT63042 features input Under-Voltage Lock-out UVLO, over current, short circuit protection, and over temperature protection.

The SCT63042 is available in a compact 2mm*2mm QFN package.

TYPICAL APPLICATION



4.85V LDO Vout vs Vin @different Iout



REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0: Production

Revision 1.1: Update DEVICE ORDER INFORMATION

DEVICE ORDER INFORMATION

ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION
SCT63042FJBR	Tape & Reel	3000	3042	18	QFN-18L

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION	MIN	MAX	UNIT
PVIN1, PVIN2	-0.3	8	V
SW1,SW2	-1	8	V
BST1,BST2	-0.3	14	V
BST1-SW1,BST2-SW2	-0.3	6	V
VDD, VDM, EN, PWM1, PWM2, ISNS, IDMO, VDMO	-0.3	6	V
Operating junction temperature TJ(2)	-40	125	°C
Storage temperature TSTG	-65	150	°C

PIN CONFIGURATION

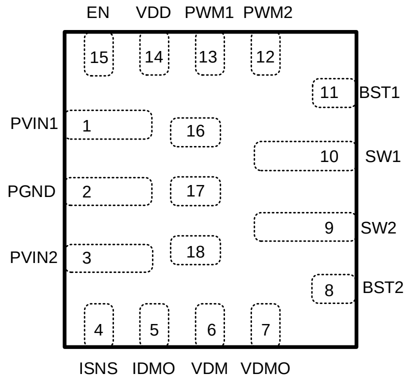


Figure 1. Top view 18-Lead QFN 2mm*2mm

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.

(2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

PIN FUNCTIONS

NAME	NO.	PIN FUNCTION
PVIN1	1,16	Input supply voltage of half-bridge FETs Q1 and Q2, VDD. Connected to the drain of high side FET Q1. a local bypass capacitor from PVIN1 pin to PGND pin should be added. Path from PVIN1 pin to high frequency bypass capacitor and PGND must be as short as possible.
PGND	2,17	PGND is the common power ground of the full bridge, connected to the source terminal of low side FETs Q2 and Q4 internally.
PVIN2	3,18	Input supply voltage of half-bridge FETs Q3 and Q4. Connected to the drain of high side FET Q3. Local bypass capacitor from PVIN2 pin to PGND pin should be added. Path from PVIN2 pin to high frequency bypass capacitor and PGND must be as short as possible.
ISNS	4	Current detection output. The voltage of the pin is proportional to the input current.
IDMO	5	Current demodulation output.
VDM	6	High-pass filter input. Voltage demodulation pin data packets based on coil voltage.
VDMO	7	Voltage demodulation output.

BST2	8	Power supply bias for the high-side power MOSFET gate driver of Q3 as shown in the block diagram. Connect a 0.1uF capacitor from BST2 pin to SW2 pin.
SW2	9	Switching node of the half-bridge FETs Q3 and Q4.
SW1	10	Switching node of the half-bridge FETs Q1 and Q2.
BST1	11	Power supply bias for the high-side power MOSFET gate driver of Q1 as shown in the block diagram. Connect a 0.1uF capacitor from BST1 pin to SW1 pin.
PWM2	12	PWM logic input to the FET Q3 and Q4 as shown in the Block Diagram. Logic HIGH turns off the low-side FET Q4, and turns on the high-side FET Q3. Logic LOW turns off the high-side FET Q3 and turns on the low-side FET Q4.
PWM1	13	PWM logic input to the FET Q1 and Q2 as shown in the Block Diagram. Logic HIGH turns off the low-side FET Q2, and turns on the high-side FET Q1. Logic LOW turns off the high-side FET Q1 and turns on the low-side FET Q2.
VDD	14	Output voltage of the 4.85V LDO. Connect 10uF capacitor from this pin to GND pin.
EN	15	Enable pin. Pull the pin high or keep it floating to enable the IC. When the device is enabled, IC will start to work if VIN higher than UVLO threshold. After VDD is established, power stage responds to PWM input logic then.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted.

PARAMETER	DEFINITION	MIN	MAX	UNIT
P_{VIN}	Input voltage range	4	6	V
T_J	Operating junction temperature	-40	125	°C

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model(HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins(1)	-3	+3	kV
	Charged Device Model(CDM), per ANSI-JEDEC-JS-002-2014specification, all pins(2)	-1	+1	kV

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

THERMAL INFORMATION

PARAMETER	THERMAL METRIC	QFN-18L	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance(1)	68	°C/W
$R_{\theta JC}$	Junction to case thermal resistance(1)	50	

(1) SCT provides $R_{\theta JA}$ and $R_{\theta JC}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JC}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT63042 is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads of the SCT63042. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual $R_{\theta JA}$ and $R_{\theta JC}$.

ELECTRICAL CHARACTERISTICS

V_{PVIN1}=V_{PVIN2}=5V, typical value is tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Input supplies and UVLO						
P_{VIN}	Operating input voltage		4		6	V
P_{VIN1_UVLO}	P_{VIN1} UVLO Threshold Hysteresis	P_{VIN1} rising		3.6 300	3.9	V mV
I_{SHDN_PVIN1}	Shutdown current from PVIN1	EN=0V, PVIN1=5V		0.5	1.2	uA
I_{SHDN_PVIN2}	Shutdown current from PVIN2	EN=0V, PVIN2=5V			0.5	uA
I_{PVINQ}	Quiescent current from PVIN1, PVIN2	EN floating, no loading on LDO		580	650	uA
ENABLE INPUTS and PWM logic						
V_{EN_H}	Enable high threshold			1.2	1.24	V
V_{EN_L}	Enable low threshold			1.1		V
V_{IH}	PWM1, PWM2 Logic level high	VDD=4.85V	2.5			V
V_{IL}	PWM1, PWM2 Logic level low	VDD=4.85V			0.8	V
$R_{pull\text{-}down}$	PWM1/2 inner pull-down Res			100		kΩ
Power Stage						
$R_{DSON\_Q1\ Q3}$	High-side MOSFET Q1 Q3 on-resistance	V_{BST1}-V_{SW1}=4.85V, V_{BST2}-V_{SW2}=4.85V		20	30	mΩ
$R_{DSON\_Q2\ Q4}$	Low-side MOSFET Q2 Q4 on-resistance	VDD=4.85V		20	30	mΩ
I_{LIM}	High-side current limit threshold		5.4	6	6.6	A
4.85V LDO						
V_{DD}	Output voltage	Cout=10uF	4.8	4.85	4.9	V
I_{DD}	Output current Capability			65		mA
Current Sense						
V_{ISNS0}	Voltage with no input current	I_{PGND}=0A, PWM1=PWM2=0V	0.58	0.6	0.62	V
R_{ISNS}	Input current to output voltage gain	V_{ISNS}=V_{ISNS0}+I_{PGND}*R_{ISNS}	1.47	1.5	1.53	V/A
Protection						
T_{SD}	Thermal shutdown threshold Hysteresis	T_J rising		155 35		°C °C

TYPICAL CHARACTERISTICS

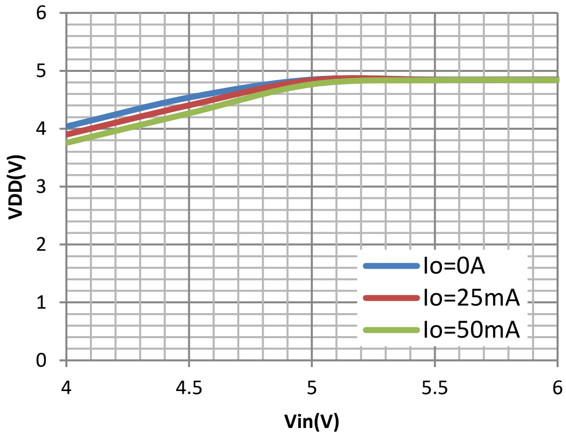


Figure 1. 4.85V LDO Vout vs Vin @different Iout

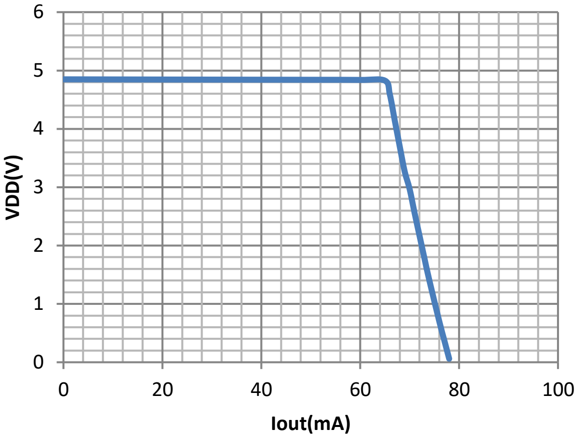


Figure 2. 4.85V LDO Vout vs Iout @Vin=6V

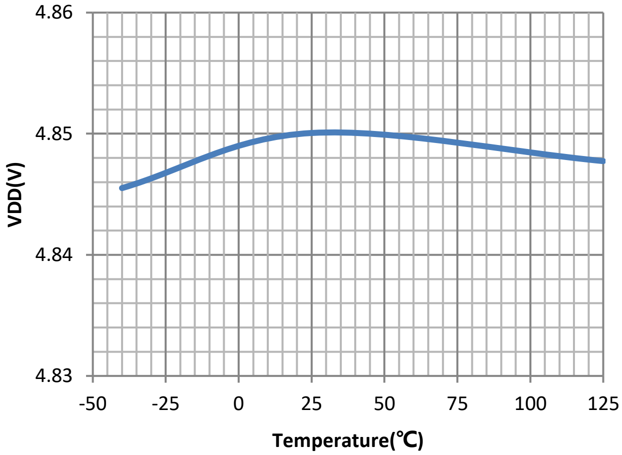


Figure 3. 4.85V LDO Vout vs temperature

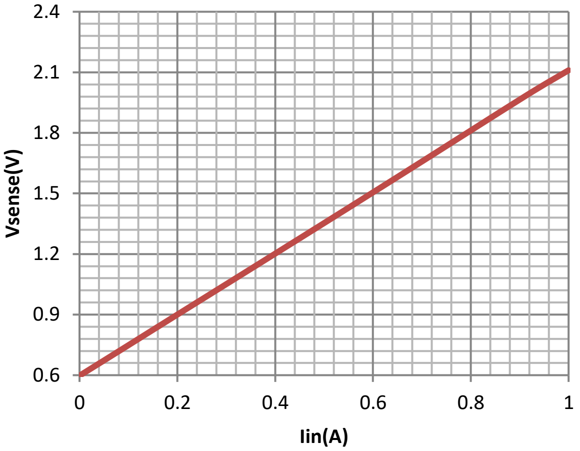


Figure 4. Current Sense Output Voltage vs Iin

FUNCTIONAL BLOCK DIAGRAM

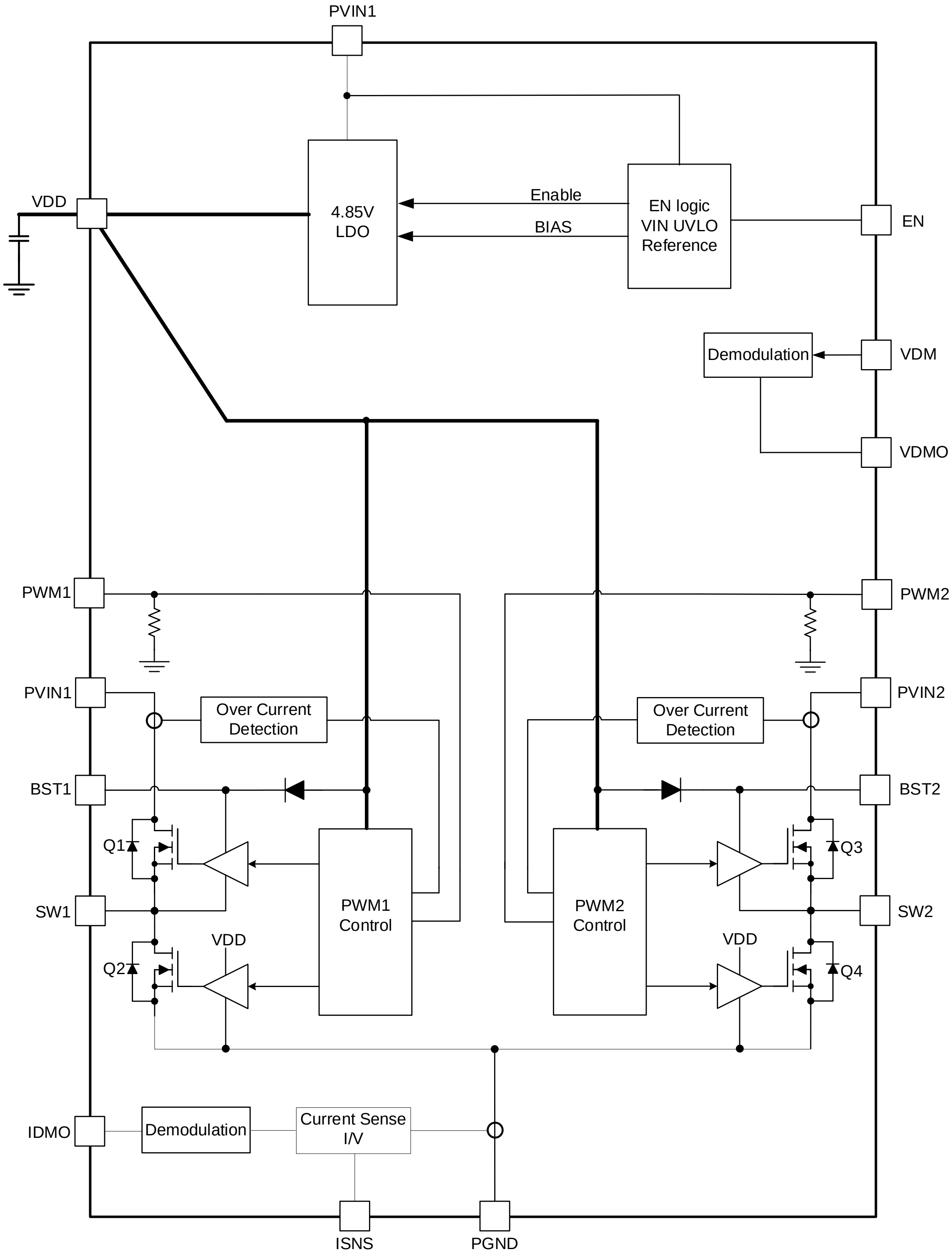


Figure 5. Functional Block Diagram

OPERATION

Overview

The SCT63042 is a highly integrated power management unit optimized for wireless power transmitter applications. This device integrates the power functions required to a wireless power transmitter including 4.85V output LDO as power supply for external transmitter controller, full bridge power stage to convert DC input power to AC output for driving LC resonant circuit, lossless current sensing with ±2% accuracy.

The SCT63042 has two power input pins. PVIN1 and PVIN2 are connected to the power FETs of the full bridge and conducts high currents for power transfer.

PVIN1, PVIN2 can be powered separately for more flexibility of system power design. The operating voltage range for PVIN is from 4V to 6V. An Under-Voltage Lockout(UVLO) circuit monitors the voltage of PVIN1 pin and disable the IC operation when PVIN1 voltage falls below the UVLO threshold of 3.3V typically. When PVIN1 voltage rise to 3.6V, VDD can start work, which is the power supply for gate drivers of full bridge MOSFETs.

Two independent PWM signals control two separate half bridge MOSFETs with internal adaptive non-overlap circuitry to prevent the shoot-through of MOSFETs in each bridge. PWM logics are compatible for both 3.3V and 5V IOs so the SCT63042 can accept PWM signal from the controller with using either 3.3V or 5V power supply.

The full bridge of power MOSFETs includes proprietary designed gate driver scheme to resist switching node ringing without sacrificing MOSFET turn-on and turn-off time, which further erases high frequency radiation EMI noise caused by the MOSFETs hard switching. This allows the user to reduce the system cost and design effort for EMI reduction.

The SCT63042 full protection features include PVIN under-voltage lockout, over current protection with cycle-by-cycle current limit and hiccup mode, output hard short protection for 4-MOSFETs full bridge, current limit and current fold back at hard short for VDD and whole chip thermal shutdown protection.

Enable and Start up Sequence

When the PVIN pin voltage rises above 3.6V and the EN pin voltage exceeds the enable threshold of 1.2V, the 4.85V output LDO enables at once, 4-MOSFETs full bridge allows PWM signal to control for switching. And the device disables when the PVIN pin voltage falls below 3.3V or when the EN pin voltage is below 1.1V. LDO disable and PWM input cannot control full bridge of MOSFETs. An internal pull up current source to EN pin allows the device enable when EN pin is floating to simply the system design.

4.85V LDO

The SCT63042 has an integrated low-dropout voltage regulator which powered from PVIN1, and supply regulated 4.85V voltage on VDD pin. The output current capability is 65mA. This LDO can be used to bias the supply voltage of external transmitter controller directly.

It is recommended to connect a decoupling ceramic capacitor of 1uF to 10uF to the VDD pin. Capacitor values outside of the range may cause instability of the internal linear regulator.

Full bridge and PWM Control

The SCT63042 integrate full bridge power stage with only 20mohm on-resistance for each power MOSFET optimized for wireless power transmitter driving the LC resonant circuit. This full bridge can operate in a wide switching frequency range from 20KHz to 400KHz for different applications which is completely compatible with WPC's frequency requirement from 100KHz to 205KHz.

PWM1 input controls the half bridge comprised of high side MOSFET Q1 and low side MOSFET Q2, and PWM2 input controls the half bridge comprised of high side MOSFET Q3 and low side MOSFET Q4 as shown in block diagram. The PWM1 and PWM2 independently control the SW1 and SW2 duty cycle and frequency. Logic HIGH will turn off low side FET and turn on high side FET, and logic LOW will turn off high side FET and turn on low side FET, PWM1 and PWM2 is default pull-down to GND by 100kΩ inner resistor.

An external 100nF ceramic bootstrap capacitor between BST1 and SW1 pin powers floating high-side power MOSFET Q1's gate driver, and the other 100nF bootstrap capacitor between BST2 and SW2 pin powers for the Q3's gate driver. When low side FET is on which means SW is low, the bootstrap capacitor is charged through internal path by VDD power supply rail.

PWM cannot been kept as high level for more than 2ms since the voltage of bootstrap capacitor will be discharged by internal leakage current if high side FET keeps on.

Full Bridge Over Current Protection

The SCT63042 integrates cycle-by-cycle current limit and hiccup mode for over-current protection. The current of the high side FET Q1 and Q3 is sensed and compared to the current limit threshold during each switching cycle. If the current exceeds the threshold, 6A typical, the high side FET turns off immediately in present cycle to avoid current increasing even PWM signal is still kept in high level. The over current counter is incremented. If one high side FET occurs over current in 5 consecutive cycles, then all 4 internal FETs are turned off regardless of the PWM inputs. The full bridge enters hiccup mode and will attempt to restart after a time-out period of 20ms typically.

Current Sense

The SCT63042 has a proprietary lossless average current sensing circuit that measures the average input current of full bridge with ±2% accuracy and reports a proportional voltage directly to the ISNS pin. This voltage information on ISNS pin can be send to specialized controller or general MCU for Foreign Object Detection FOD and current demodulation.

When the full bridge of MOSFETs does not work, no current flows to PGND. The DC bias voltage on ISNS pin is 600mV.This DC bias helps set up a suitable voltage bias for the following analog to digital converter in MCU or amplifier for current demodulation. The average input current to voltage conversion gain on ISNS is 1.5V/A. The equation 1 represent the corresponding relation for the output voltage on ISNS pin and average current to PGND from full bridge.

$$\mathrm{V_{ISNS}} = 600\mathrm{mV} + \mathrm{I_{PGND}} * 1.5\mathrm{V/A} \qquad (1)$$

Voltage and Current Demodulation

The SCT63042 integrates two demodulation schemes, one based on coil voltage information calling voltage demodulation and the other based on input average current information calling current demodulation.

The voltage mode envelope detector is implemented using a discrete solution as depicted on Figure6. This simple implementation achieves the envelope detector function, low-pass filter as well as the DC filter function. The envelope detector applies the analog signal to VDM pin and the chip do the demodulation and output a digital signal to VDMO pin which MCU can capture the voltage demodulation results and then implement the packet decode.

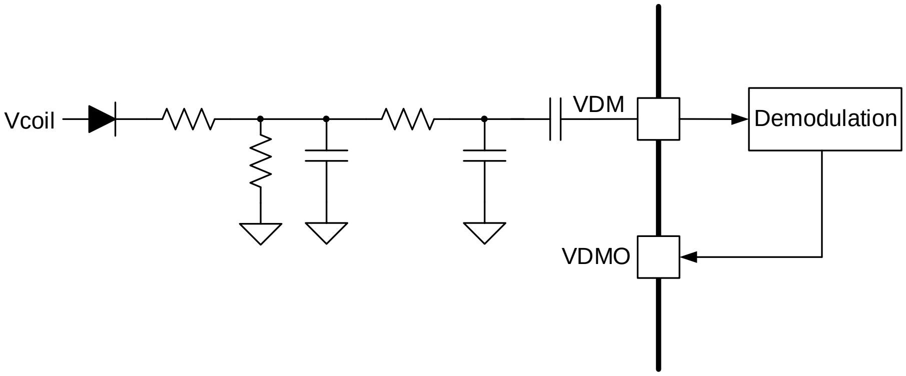


Figure 6. Envelope Detector

APPLICATION INFORMATION

Typical Application

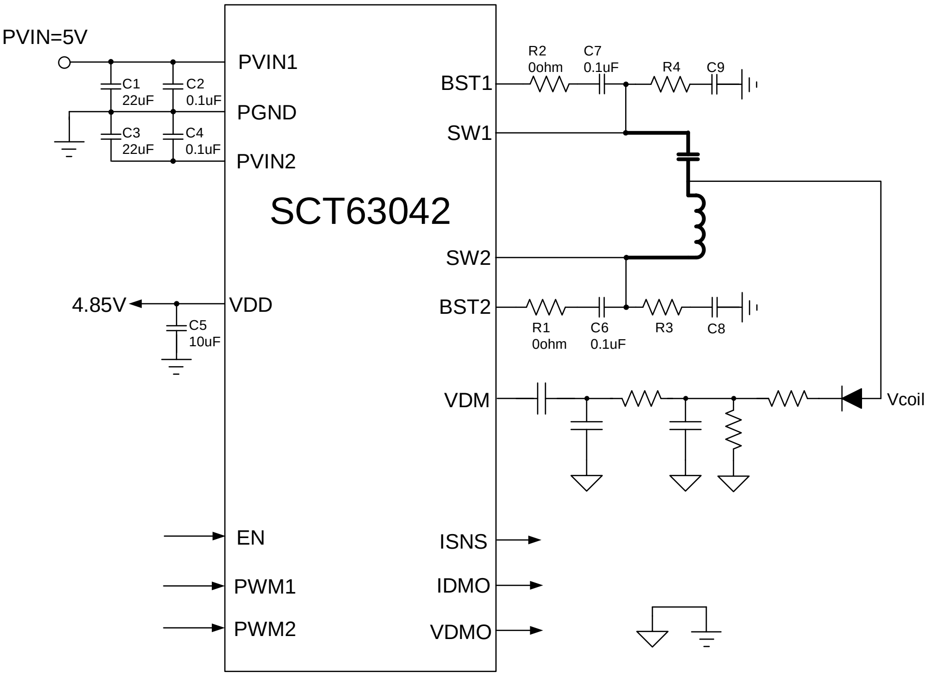


Figure 7. Same Input to PVIN

Application Waveforms

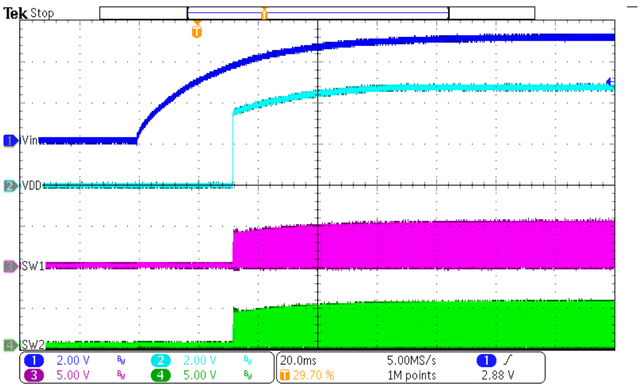


Figure 8. Power Up

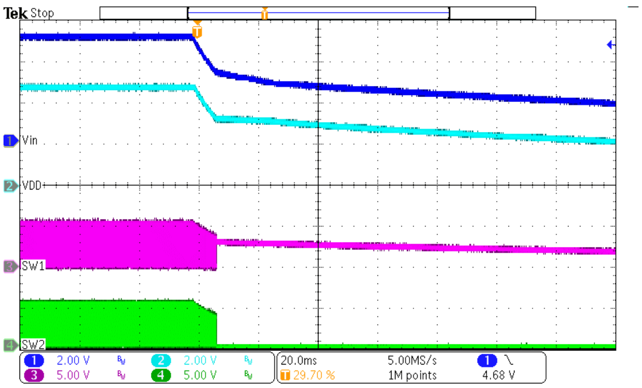


Figure 9. Power Down

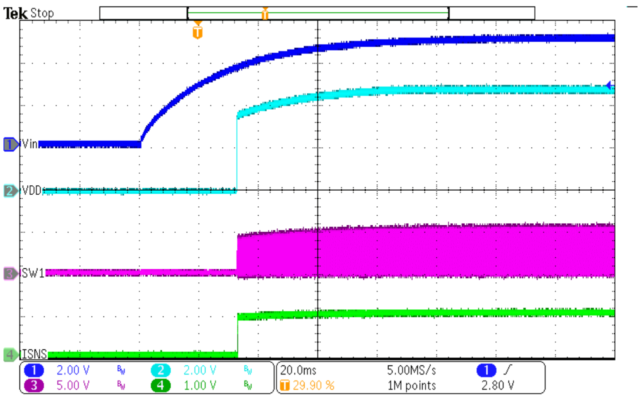


Figure 10. Power Up

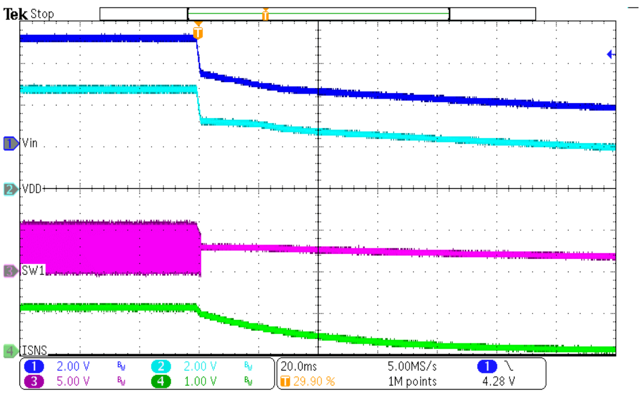


Figure 11. Power Down

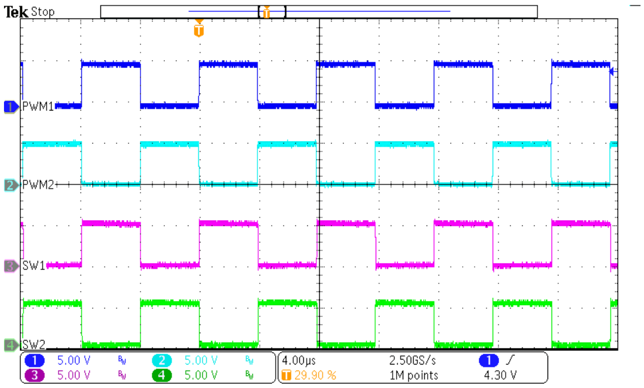


Figure 12. Full bridge @Vin=5V, RX=5W

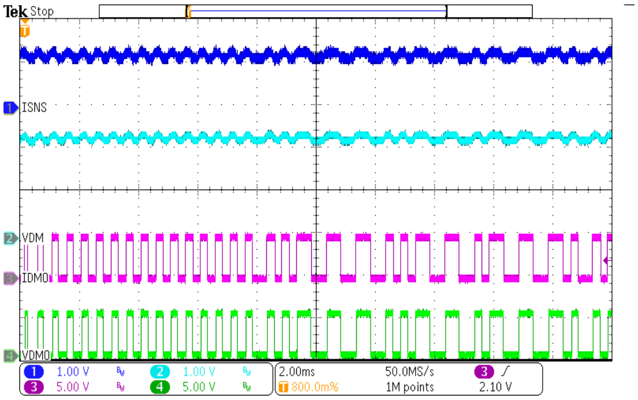


Figure 13. VDMO/IDMO Demodulation Output

Layout Guideline

Proper PCB layout is a critical for SCT63042's stable and efficient operation. For better results, follow these guidelines as below:

1. Bypass capacitors from PVIN to PGND should put next to PVIN and PGND pin as close as possible especially for the two small capacitors.
2. PGND connect to bottom layer by via between capacitors.
3. Bypass capacitor for VDD place next to VDD pin.

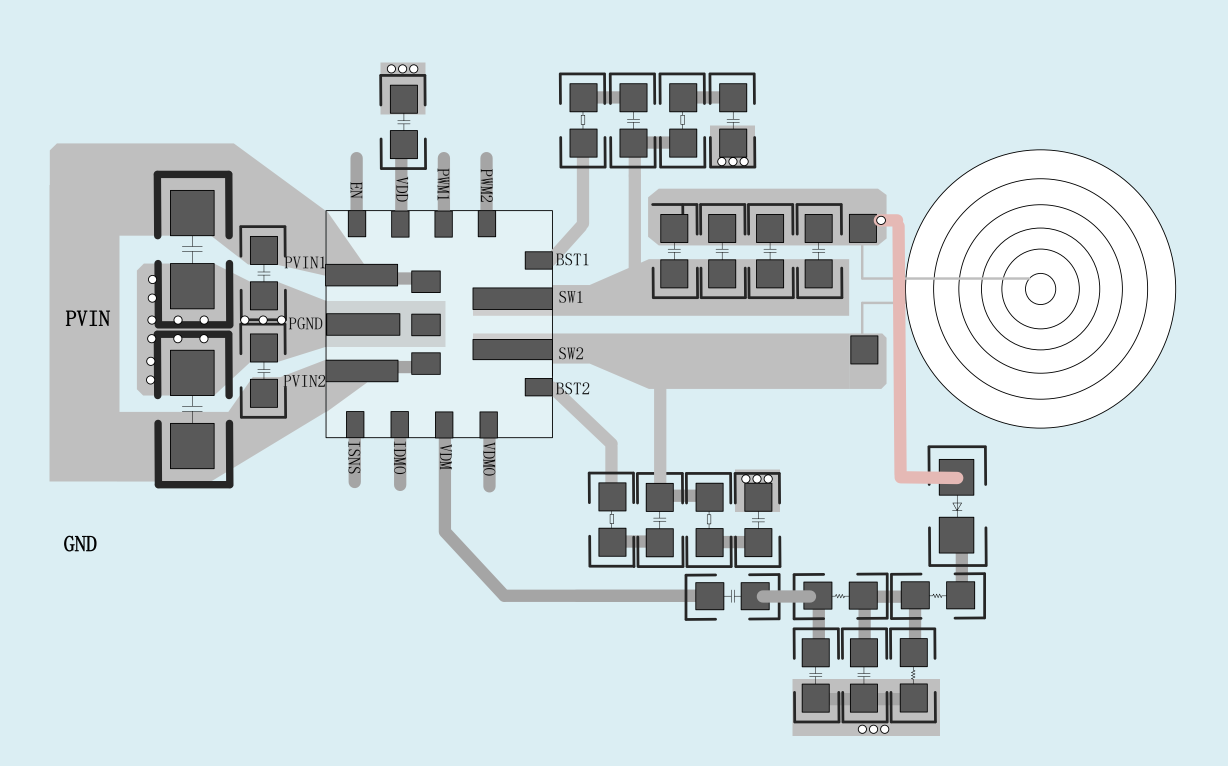
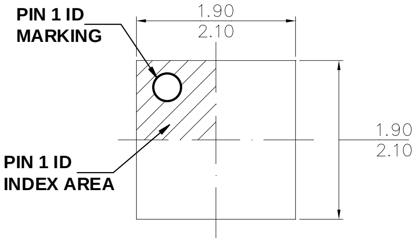


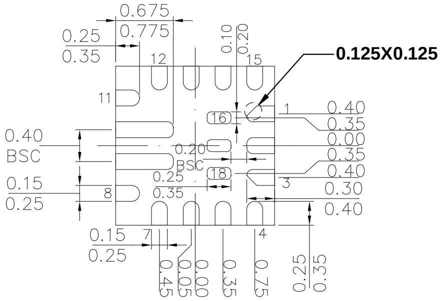
Figure 14. PCB Layout Example

PACKAGE INFORMATION

QFN -18L (2mm x 2mm)

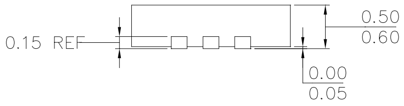


TOP VIEW

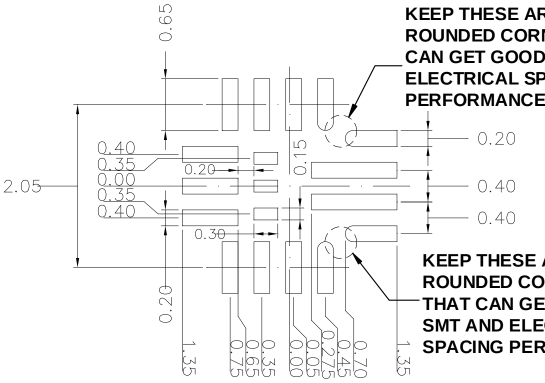


0.125X0.125

BOTTOM VIEW



SIDE VIEW



KEEP THESE AREAS AS ROUNDED CORNERS THAT CAN GET GOOD SMT AND ELECTRICAL SPACING PERFORMANCE

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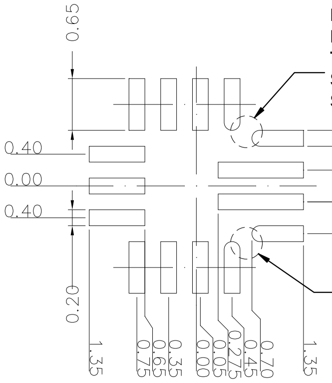
RECOMMENDED LAND PATTERN PLAN A



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RECOMMENDED LAND PATTERN PLAN B

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) RECOMMENDED LAND PATTERN PLAN B IS FOR THOSE CUSTOMERS WHO DON`T HAVE 0.15MM PIN WIDTH PCB&SMT CAPABILITY.
5) DRAWING IS NOT TO SCALE.

APE AND REEL INFORMATION